CANBERRA

Model 2037A
Edge/Crossover SCA

User's Manual

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EDGE/CROSSOVER TIMING SCA
MODEL 2037A

CONTENTS

EDGE/CROSSOVER TIMING SCA
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Section 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The Canberra Model 2037A EDGE/CROSSOVER TIMING Single Channel Analyzer performs both energy and timing analysis on analog pulses from nuclear pulse shaping amplifiers. Energy analysis is derived by discrimination of the peak amplitude of the input energy pulses, and timing is derived by discrimination of a fixed amplitude reference for the leading edge mode, or the true zero crossing of a bipolar waveform for the crossover mode. A front panel MODE switch allows selection of either timing derivation.

The leading edge technique finds best application to fast-shaped unipolar signals of a fairly narrow energy (pulse height) range. The crossover technique exploits the amplitude insensitive zero voltage crossing of a bipolar pulse to provide stable timing reference for a broad energy range.

1.2 ENERGY ANALYSIS

The logic output (SCA) is provided as both positive and negative NIM-level pulses for each input analog pulse whose peak amplitude is between the levels determined by the front panel ten-turn dial controls. The pulse peak must exceed the LOWER LEVEL (E) reference, but not exceed the sum of the LOWER LEVEL (E) + WINDOW (Δ E) reference to generate the SCA output.

The SCA output may be used to assist in a wide variety of conventional applications from simple noise stripping to extraction of a narrow energy range from a wide spectrum for detailed spectroscopy.

Energy discrimination in the Model 2037A, is sharp, precise and stable. Temperature drift of the discrimination thresholds, for example, is less than $\pm$ 0.005%/^{o}C ($\pm$ 50ppm/^{o}C) of full scale. The energy discriminators are DC coupled at the input to allow excellent baseline stability limited only by the shaping amplifier's restorer. These significant features permit excellent amplitude discrimination, even in high count rate spectra.

The LOWER LEVEL (E) threshold is calibrated by reference to the regulated NIM supply voltages, and is usable in a range from + 0.1VDC to + 10.0VDC. Linearity of control is limited only by the specified $\pm$ 0.25% maximum integral nonlinearity of the front panel dial potentiometer.

The WINDOW (Δ E) threshold is also calibrated by reference to the regulated NIM supply voltages, and is usable in a range from the LOWER LEVEL (E) setting to + 10.0VDC. A front panel Δ E RANGE switch allows use of a 1.0 volt full scale range for very fine adjustments of a small energy window.

1.3 TIMING ANALYSIS

For the leading edge mode, a true low level leading edge technique is employed to minimize timing jitter. To simplify setup and adjustment, the threshold level for the leading edge timing discriminator is set to track the LOWER LEVEL (E) control at 50%, up to a limit of 200mVDC. For reasonably large input pulse heights, then, timing is referenced to the 200mVDC level. To simplify adjustment of timing dwell for the risetime of the input pulse, that function has been incorporated in an extended range DELAY control. The user can simply set the selected delay for the known time-to-peak of the input pulse (or at least 2x the shaping time constant used in a semi-Gaussian pulse) without the need for tedious oscilloscope trimming.

For the crossover mode, a bridge circuit timing discriminator is used to sense the true zero crossing of the bipolar energy pulse as superimposed on a DC offset of up to ± 100mVDC. A front panel WALK ADJustment is provided to trim walk over the dynamic range used.

One important design feature of the Model 2037A is the pulse lock-out logic for the crossover mode. First, internal gating prevents the timing cycle (including the front panel selected DELAY) from being initiated on events below the selected LLD threshold, and thus minimizes dead time. Events recognized above the ULD are accepted and processed through the full timing cycle so that the ULD can provide timing data. Secondly, the lock-out logic rejects energy pulses which arrive after the first valid signal (i.e., above the LLD) but prior to reset at the end of a normal timing cycle. This prevents a second, possibly higher energy signal from changing the data latches and causing an erroneous output (timed to one event and energy gauged to a second). Thirdly, the lock-out logic prevents timing aberrations due to pileup by responding only to the next full event following a timing cycle instead of the potentially long tail of a pulse arriving at or near the end of one timing cycle. These features enhance the performance of the unit in the crossover mode by eliminating the pulse ambiguities described. Unfortunately, the same lock-out logic cannot be used to prevent potentially erroneous outputs in the leading edge mode.

The pulse outputs may be delayed by up to 11μsec relative to a prompt output by use of the front panel linear DELAY control. Two ranges are provided: 0.1-1.1μsec, and 1-11μsec. The selected delay and the output pulse width plus reset time determine the pulse pair resolution under any given circumstances. Optimum performance is about 800nsec unless a shorter positive output pulse is acceptable.

1.4 OUTPUT OPTIONS

The positive output logic signal is adjustable in peak amplitude for compatibility with interfacing instruments. The output is source-matched with a 50 ohm series resistive termination to prevent ringing due to reflections on unterminated cables, and the resulting multiple counting frequently experienced. The instrument is shipped with a socketed resistor which limits the output to + 5V nominal (open circuit) for direct interface with common TTL circuitry. The user may remove the resistor to obtain a + 8V nominal open circuit voltage for instruments requiring the NIM pulse level, or + 4V nominal into the 50 ohm load termination which some other instruments provide. This flexibility allows the user to adapt the output signal to his needs without risking the problems encountered with improperly driven cables and critical timing pulses.

The negative SCA output is a NIM standard 16mA current pulse designed to yield a nominal - 800mV pulse across a 50 ohm load termination. Source matching here again guarantees a clean, stable pulse output even with a load mismatch, if that becomes desirable.

Careful attention has been paid to minimize reflections of the fast logic pulses onto the analog input. Thus all logic outputs are isolated from chassis to prevent circulating pulse currents in the instrument Bin.

Section 2
SPECIFICATIONS

2.1 INPUTS

SIGNAL INPUT	Accepts + 0.1 to + 10.0VDC, unipolar or bipolar (positive lobe leading) pulses from shaping amplifier. DC coupled. Input impedance 1K ohms. Shaping time constant range 0.1 to 10 microseconds. Front panel BNC connector. Front panel test point.

2.2 OUTPUTS

SCA (+)	Positive logic + 5V nominal pulse amplitude. Output impedance 50 ohms. Pulse width 0.5 microseconds nominal; rise time and fall time less than 25 nanoseconds. Front panel BNC. Front panel test point.
SCA (-)	Negative logic – 16mA current pulse (current sinking). Output impedance 50 ohms. Pulse width 20 nanoseconds nominal; rise time less than 5 nanoseconds. Front panel BNC. Front panel test point.

2.3 PERFORMANCE

DISCRIMINATOR NONLINEARITY	Less than ± 0.25% of full scale for either LOWER LEVEL (E) or WINDOW (Δ E).
DISCRIMINATOR STABILITY	Better than ± 0.005%/°C (± 50ppm/°C) of full scale, referenced to NIM class A supply + 24.0VDC line.
DISCRIMINATOR RANGE	100:1 (0.1 to 10.0VDC).
DELAY NONLINEARITY	Less than ± 1% of full scale.
DELAY STABILITY	Better than ± 0.01%/°C (± 100ppm/°C).
PULSE PAIR RESOLUTION	Limited by output pulse width (positive) plus delay selected, plus 200 nanoseconds cycle time. Minimum resolving time 800 nanoseconds (with 0.1 microsecond shaped input).
WALK	Referenced to a + 10.0V full scale input. A) For leading edge mode: with risetime less than 100 nanoseconds:

DYNAMIC RANGE	WALK (MAX.)
10:1	± 40 nanoseconds
50:1	± 100 nanoseconds

B) For Crossover mode: with bipolar input pulse with 0.5 microsecond shaping:

DYNAMIC RANGE	WALK (MAX.)
10:1	± 2 nanoseconds
50:1	± 4 nanoseconds

C) For crossover mode, with DDL shaped input (1μsec delay line, rise time less than 100nsec):

DYNAMIC RANGE	WALK (MAX.)
10:1	± 1 nanoseconds
50:1	± 2 nanoseconds

Walk beyond a 100:1 range is limited by jitter due to amplifier noise effects. Detector and system noise, and other baseline anomalies, may restrict usable dynamic range for timing analysis purposes in a given experimental setup to less than those quoted above.

2.4 CONNECTORS

All inputs and outputs are by BNC, type UG-1094/U connectors. Output connectors are isolated from chassis.

2.5 POWER REQUIREMENTS

+24VDC	:	30mA
- 24VDC	:	10mA
+12VDC	:	145mA
- 12VDC	:	55mA

2.6 PHYSICAL

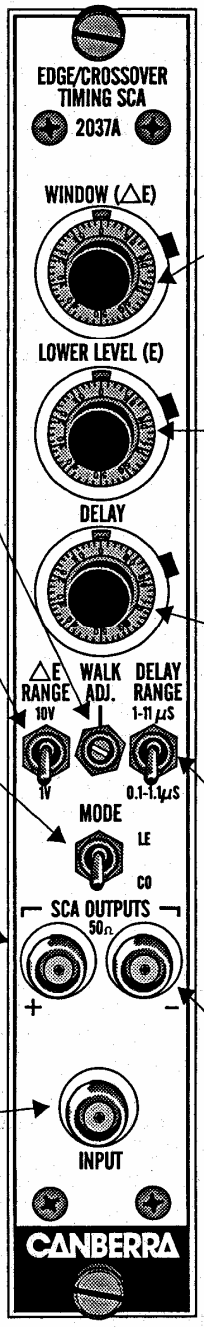
SIZE — Standard single width Nuclear Instrument Module (NIM), (1.35 x 8.714 inches), (3.43 x 22.13cm) per TID-20893 (rev.).

NET WEIGHT — Approximately 2.5 lbs. (1.15 kg.).

Section 3
CONTROLS AND CONNECTORS

This section describes the function of the controls, and the adjustments which the user can make, in the Model 2037A EDGE/CROSSOVER TIMING SCA. It is recommended that this section be read before proceeding with operation of the instrument.

3.1 FRONT PANEL CONTROLS



WALKADJ
Screwdriver trim potentiometer to adjust time walk.

Δ E RANGE
Toggle switch to set full scale range of WINDOW (Δ E) control as 1.0 or 10.0 V dc.

MODE
Two position toggle switch to select either leading edge (LE) or crossover (CO) timing mode.

SCA OUTPUT (+)
Provides +5 V output pulse for each analog input pulse meeting SCA energy level requirements.

INPUT
Accepts 0.1-10 V dc peak pulses from nuclear pulse shaping amplifier for energy and timing analysis. Input impedance 1 k ohms.

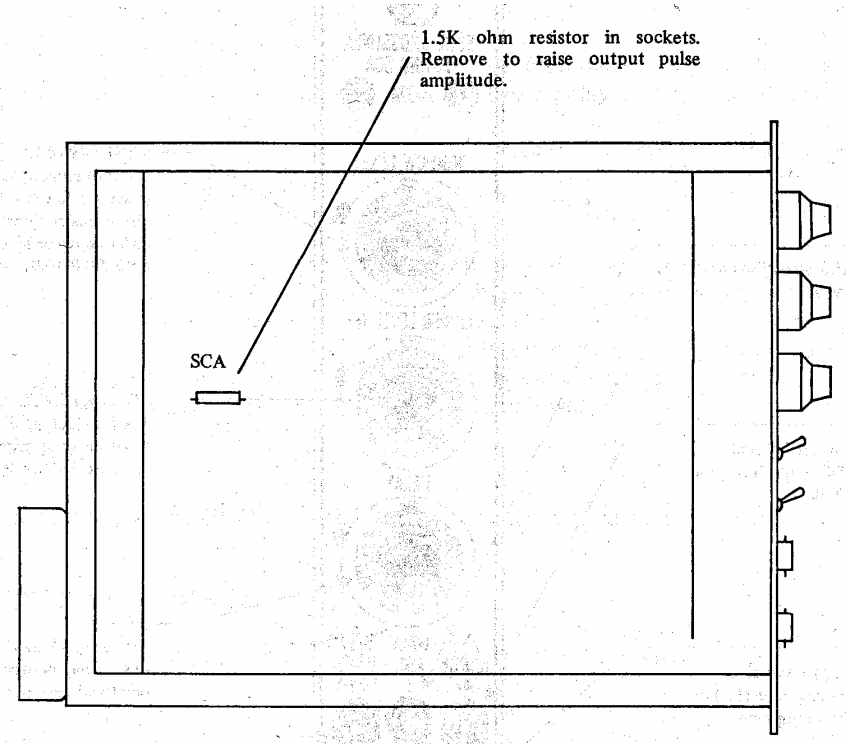
WINDOW (Δ E)
Ten turn locking dial potentiometer to set window width (upper discriminator threshold level, added to lower level). Scaled 0.0-10.0 V dc.

LOWER LEVEL (E)
Ten turn locking dial potentiometer to set lower discriminator threshold level. Scaled 0.1-10.0 V dc.

DELAY
Ten turn locking dial potentiometer to set delay between prompt timing point and desired output.

DELAY RANGE
Toggle switch to set full range of DELAY control as 1.1 μs or 11 μs.

SCA OUTPUT (-)
Provides -16 mA current pulse output for each analog input pulse meeting SCA energy level requirements.



The trimming potentiometers internal to the instrument are carefully calibrated during factory test to provide the precise lower end and full scale limits for the front panel controls. The user should normally have no need to readjust these, but if adjustments are necessary the setup and general procedure given in Section 4 should be followed. The trimming functions are:

RV1:	Low end limit trim for WINDOW (Δ E)
RV2:	Transfer gain trim, LOWER LEVEL (E) to WINDOW (Δ E)
RV3:	High end limit trim for WINDOW (Δ E), 0-10V
RV4:	High end limit trim for WINDOW (Δ E), 0-1V
RV5:	Low end limit trim for LOWER LEVEL (E)
RV6:	High end limit trim for LOWER LEVEL (E)

The adjustment for output pulse voltage level is made with the socketed 1.5K ohm resistor as illustrated. With the resistor installed, the output pulse is clamped at + 5VDC nominal, open circuit. With the resistor removed, the output pulse voltage will be + 8VDC open circuit, and + 4VDC nominal into a 50 ohm load.

Section 4
OPERATING INSTRUCTIONS

The purpose of this section is to familiarize the user with the Model 2037A EDGE/CROSSOVER TIMING SCA, and to check that the unit is operating correctly. Since it is difficult to determine the exact system configuration in which the unit will be used, explicit operating instructions cannot be given. However, if the following procedure is carried out, the user will gain sufficient familiarity with this instrument to permit its proper use in the system at hand. Additionally, if operating difficulties cause the user to suspect the proper functioning of the instrument at any time, this procedure will exercise the controls and operating modes such as to confirm proper functioning or to help isolate a malfunction.

4.1 DISCUSSION OF MEASUREMENT TECHNIQUES

There are two key measurements involved in checking the normal operation of a precision nuclear instrument such as the Model 2037A that can be distorted or even masked by improper measurement techniques: that setting the precise thresholds of energy discrimination, and that observing and/or trimming the time walk.

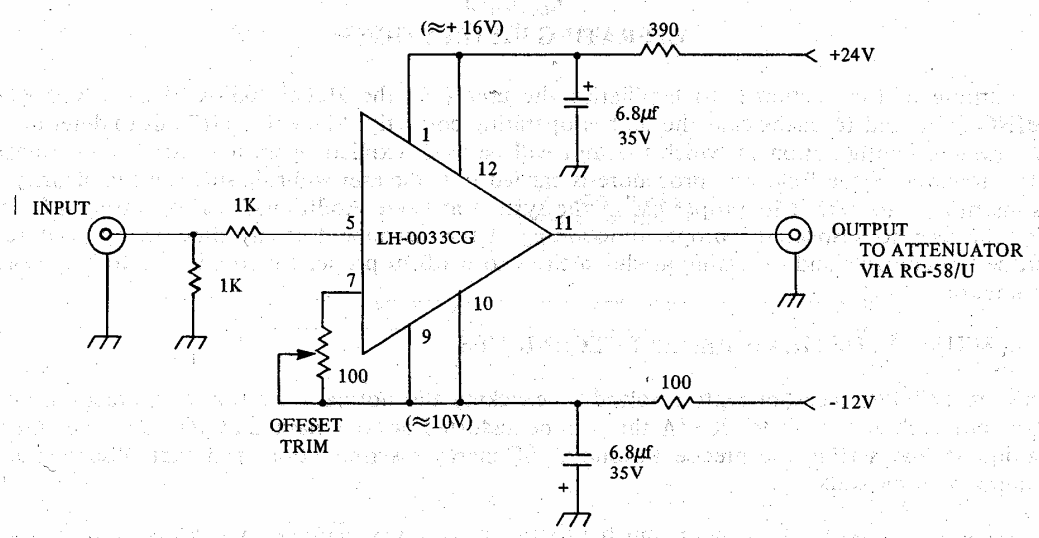
The upper and lower limits of the LOWER LEVEL (E) and WINDOW (Δ E) dial potentiometer ranges have been carefully calibrated in factory test. The precision of the examination to be described will be limited by the calibration of the user's oscilloscope. Hence, adjustments of the internal trimpots should not be attempted without a more exacting test technique. This examination will nonetheless familiarize the user with the operating range and the sharpness of discrimination and reveal malfunctions if they develop.

Regarding the walk measurements, the user must understand some subtle effects that will influence the apparent behavior of the instrument. First, when making a characterization of the instrument, the test signal amplitude must be constant at the output of the shaping amplifier and attenuation must be performed between the shaping amplifier output and the TIMING SCA input. Without this simple precaution the observed walk will include that of both amplifier and TIMING SCA and the results will vary from amplifier to amplifier. The reason for this phenomenon is that the amplifier does exhibit some walk and a slight change in precise pulse shaping as the input signal amplitude changes because of slewing effects in the gain and pulse shaping stages. While the setup and trim of a complete system must absorb and compensate this effect by adjustment of the TIMING SCA walk control, characterization or measurement of the walk of the TIMING SCA itself is obviously distorted without such a procedural correction.

Secondly, the best attenuators for these precise timing measurements are 50 ohm attenuators, of either "T or "Π" configuration. Higher impedance attenuators (e.g., 93 ohm) do not demonstrate adequate band-width and are observed to add up to a few nanoseconds of walk by themselves with various attenuation ratios. Acceptable 50 ohm attenuators include the Kay 430 series or equivalents with band widths of 1GHz or better. Precise terminations are highly recommended.

Thirdly, common nuclear shaping amplifiers are not rated to drive the required 10.0V or better output linearly to a 50 ohm load, and in fact demonstrate clipping and anomalies in pulse shaping due to loading effects on the loop gain of the output amplifier (which is commonly a final integrator).

This subtlety is induced by the attenuator impedance requirements and is not immediately apparent. Resolving this difficulty involves using a broad band buffer amplifier which will drive the 50 ohm attenuator. Such a circuit is fortunately available in the National Semiconductor LH-0033 CG. The circuit below illustrates one configuration that can be powered from the available NIM regulated power supply voltages, and has been found to yield excellent results.



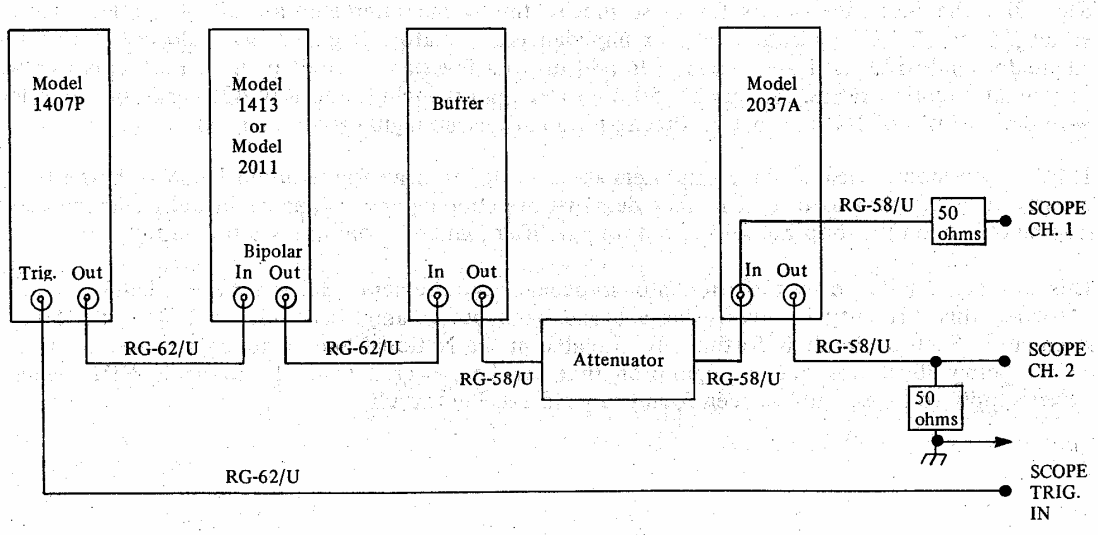
Using this procedure the TIMING SCA walk can be measured and trimmed properly. Extending the procedure, the user can then of course evaluate the relative walk behavior of several different amplifiers by substitution.

4.2 INITIAL SETUP

In order to perform the bench checkout procedure detailed below, the following equipment (or equivalents) will be required:

Canberra Model 2000 Bin/Power Supply
Canberra Model 1407P Pulse Pair Generator
Canberra Model 1413 or 2011 Spectroscopy Amplifier
Calibrated dual trace 100MHz oscilloscope (Tektronix 454, 475, etc.)
Attenuator, 50 ohm (Kay 432D, etc.)
Terminators, 50 ohm BNC

Install the Model 2037A, 1413 or 2011, and 1407P in the Bin with the power initially OFF.

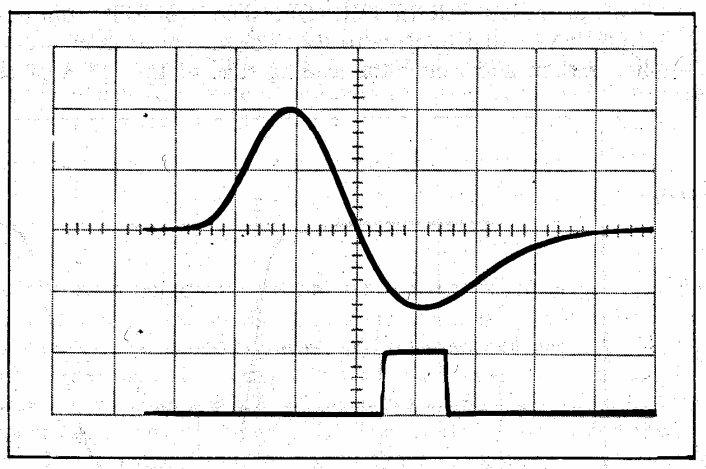


Reference control settings:

Model 1407P	RATE: Variable full CW Range 1-10KHz AMPLITUDES: full CW MODE: dual pulse ATTENUATION: out
Model 1413	* COARSE GAIN: x30 * FINE GAIN: (see below) * SHAPING: 0.5μsec * POLARITY: positive RANGE: 10V RESTORER: low
For Model 2011, same as above *	
Model 2037A	WINDOW (Δ E): 10.0 LOWER LEVEL (E): 0.1 DELAY: 0.5 Δ E RANGE: 10V DELAY RANGE: 0.1-1.1μsec MODE: CO
ATTENUATOR	all switches out
SCOPE	Channel 1: 5V/div Channel 2: 5V/div Time base: 1μsec/div, externally triggered

4.3 INITIAL CHECKOUT

Apply power to the Bin, and increase the amplifier output (FINE GAIN control) slowly to 10V peak, or just below the threshold of extinguishing the SCA output pulse as shown in the photo below. (NOTE: It is advisable for the user to verify that the Bin voltages are correct: ± 12.0VDC and ± 24.0VDC).



1. Now apply 6dB attenuation to the input signal, and adjust the WINDOW (Δ E) control to display 1.0. The SCA output pulse will be extinguished.

2. Increase the LOWER LEVEL (E) (rotate the control clockwise) until the SCA output pulse just reappears. The LOWER LEVEL (E) control dial should now display 4.00 ± 0.03. If the threshold is beyond these limits, the source of error may be in the DC level at the amplifier output or the 10V full scale level set above.

3. Now increase the setting of the LOWER LEVEL (E) control again until the SCA pulse extinguishes. The LOWER LEVEL (E) control dial should now display 5.00 ± .03.

4. Change the Δ E RANGE switch to 1V. Reduce the setting of the LOWER LEVEL (E) control to about 4.5 and raise it again slowly until the SCA output pulse just reappears. Now the control dial should display 4.90 ± 0.03.

5. Now again increase the setting of the LOWER LEVEL (E) control until the SCA pulse extinguishes. The LOWER LEVEL (E) control dial should now display 5.00 ± .03.

   These tests demonstrate the functioning of the two discriminator thresholds in determining a wide or narrow window SCA logic output.

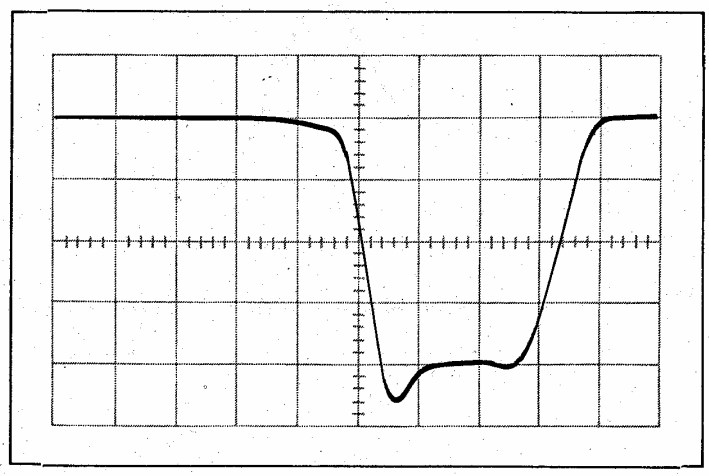
   As the Model 2037A has been carefully calibrated in factory test, the precision of this casual examination is limited by the calibration of the user's oscilloscope. The instrument may be exercised over its full rated range with this setup if the user wishes, but adjustments of internal trimports should not be attempted without a more exacting test technique.

6. For walk evaluation, it is best to view the fast leading edge of the - SCA front panel output. a 50 ohm termination should be added at the scope input connector.

   The cable connections illustrated above, and the terminations as shown, are particularly important when attempting to observe the walk characteristics of the instrument. Reflections from improperly terminated cables change the shaped pulse significantly enough to cause timing distortions by altering the constant fraction ratio.

   Best viewing of the - SCA output pulse may be had by selecting channel 2 display only, with the leading edge centered in the scope graticule. Use the delayed, expanded sweep mode to obtain a display time base of 5nsec/div. Time walk is now seen as a movement of the leading edge leftware (-) or rightward (+) as the input signal is attenuated.

   Set the front panel LOWER LEVEL (E) dial control to its counterclockwise minimum, and the WINDOW (Δ E) dial control to its clockwise maximum. Remove the 6dB attenuation step applied earlier, and center the leading edge of the - SCA pulse in the display as shown below.

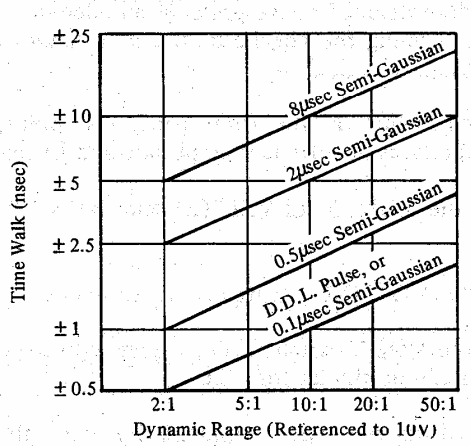


Apply a 6dB (x2) attenuation step, and verify the walk to be less than ± 1nsec from center. Adjust the front panel WALK ADJustment potentiometer if necessary.

Next successively add or change to 20dB (x10), and 34dB (x50) attenuation. Walk should be within ± 4 and ± 8nsec respectively.

The user may note that if he adjusts the walk to be 0 at the end points (e.g., at 0 and 34dB attenuation), the walk behavior at intermediate steps should still be within the specified limits (e.g., less than ± 8nsec). With proper setup and the specified equipment, the walk is typically less than 1/2 the guaranteed limits and is progressive with attenuation.

The walk behavior of the Model 2037A for other than the 0.5μsec shaping used in this test is illustrated in the chart below.



The user should realize that at longer shapings, the effects of noise and slower pulse risetimes will cause more uncertainty in precise discrimination and therefore cause jitter in the output timing. Higher amplifier gain settings likewise are responsible for jitter aggravation which may limit the usable dynamic range to somewhat less than the capability of the instrument.

7. The use of the DELAY control and the DELAY RANGE switch on the front panel are straightforward. The delay may be demonstrated by using the delayed sweep mode on the oscilloscope and lining up the leading edge of the output being observed with the left end graticule of the scope face, with the DELAY control set to minimum. Clockwise rotation of the dial will add a delay (the trace now moves to the right) linearly proportional to the dial setting for its 0.1-1.1 range.

4.4 APPLICATIONS

TIME WALK

The initial checkout procedure detailed above examines the time walk behavior of the TIMING SCA by maintaining a constant signal level in the amplifier. When the instrument is used in a typical spectroscopy system, of course, this is not the case, and the walk behavior of the amplifier must now be compensated for best experimental results. The user must again be cautioned in attempting this adjustment: the capacitive input characteristic of the pulse shaping amplifier will cause serious time walk errors when the attenuator drives the amplifier. The subtlety here is that the output impedance of the attenuator, when driven by a low source impedance, changes with attenuation and leads to pulse shape aberrations in the amplifier.

Correct procedure suggests that the attenuator (again it must be a 50 ohm type) be placed between a pulse source and the detector preamplifier test input, with that input padded to present a 50 ohm net resistive load impedance to the attenuator. The preamplifier then presents a fixed output impedance to the amplifier, and the various sources of walk can then be best compensated together. Again to minimize jitter effects, it is advisable to use as high a test signal level as can be handled linearly in the preamplifier.

Recognizing these details which influence proper alignment, the knowledgeable user can achieve best timing performance with a minimum of setup effort, using either an oscilloscope directly or a Multi-Channel Analyzer as his needs dictate.

TROUBLESHOOTING

The initial checkout procedure detailed above provides an adequate check of the basic functioning of the instrument. If after performing the checkout, the user cannot obtain the expected outputs, he should:

a) with an oscilloscope on the front panel test point, check that the input signal is received properly, is of sufficient amplitude and DC base;

b) verify that the LOWER LEVEL (E) and WINDOW (Δ E) dial controls are set as intended;

c) verify that the Δ E RANGE switch is set as intended;

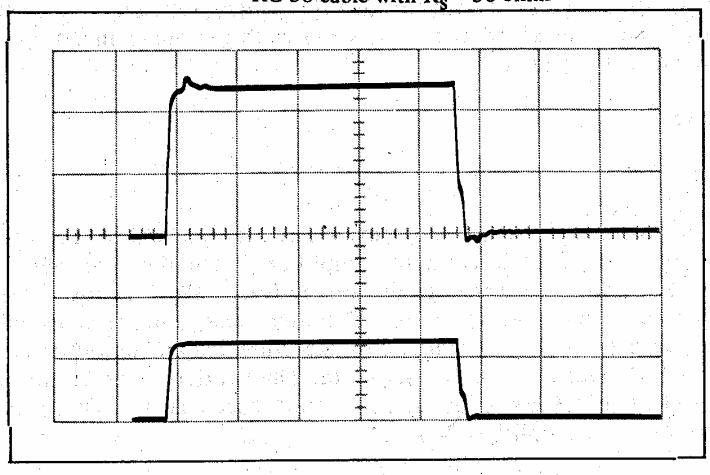
d) verify that the MODE switch is set to agree with the shaping selected on the Amplifier (unipolar for LE, or bipolar for CO).

Most difficulties are related to the user's unfamiliarity with the functions and ranges of the instrument's controls.

4.5 REFERENCE DATA ON CABLES

The following photos depict a typical output pulse at the load end of the designated RG-58/U cable and the samy point using RG-62 cable. In each case, the photographs illustrate high impedance (1K ohm) and 50 ohm termination conditions. Clearly the fastest, cleanest pulse is realized with the RG-58/U cable. With the source match provided, loading effects are limited to amplitude changes only. RG-58/U cable is therefore recommended for best compatibility with the LLD, ULD and SCA outputs.

RG-58 cable with R_S = 50 ohms:

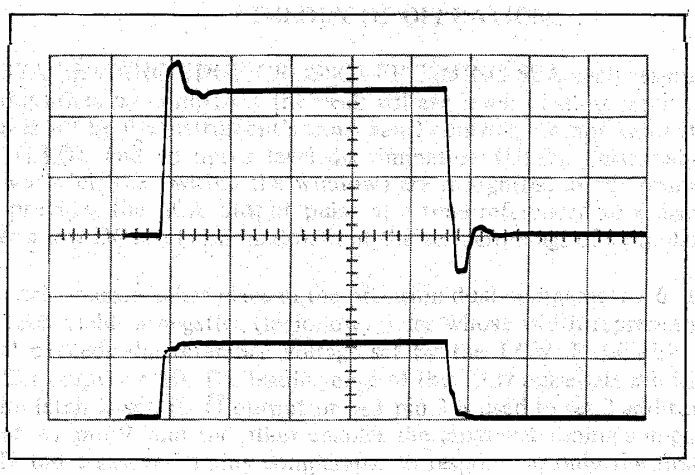


R_L = 1K ohms

R_L = 50 ohms

Horiz.: 0.1μsec/div

RG-62 cable with R_S = 50 ohms:



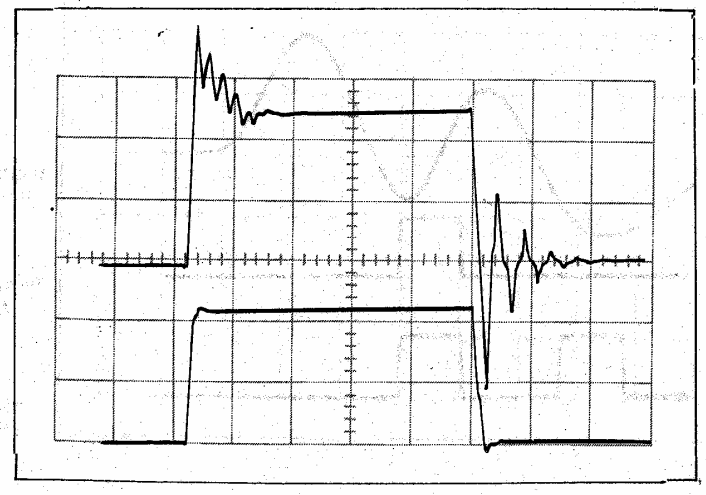
R_L = 1K ohms

R_L = 50 ohms

Horiz.: 0.1μsec/div

The picture below illustrates the same pulses with a source mismatch caused by driving the cables with the transistor switches directly. The waveforms indicate how important and effective source matching is in eliminating instabilities which cause phenomena such as multiple counting or triggering. For this reason the Model 2037A provides source matched outputs, and load end terminations are not necessary.

RG-58 or RG-62 cable driven directly:



R_L = 1K ohms

R_L = 50 ohms

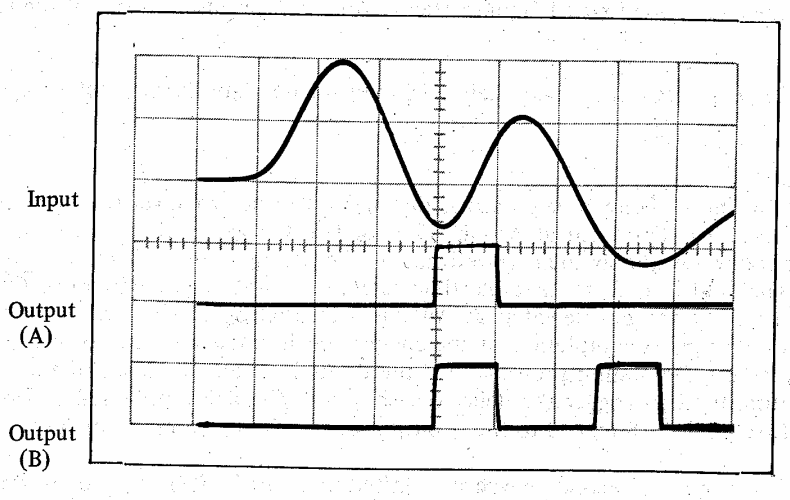
Horiz.: 0.1μsec/div

Section 5
THEORY OF OPERATION

The Model 2037A LEADING EDGE/CROSSOVER TIMING SCA analyzes nuclear energy pulses from spectroscopy amplifiers by comparing the peak voltage levels of those input pulses against stable D.C. reference voltages set by the instrument's front panel controls. Comparisons are made for a lower level discrimination (LLD), and an upper level discrimination (ULD). Pulses whose peak amplitude lies between the two levels (i.e., within the window) are recognized as the primary or SCA output. The Model 2037A provides the SCA output pulse at a time referenced to a discrimination point that is derived at either a low DC level (LE mode), or at the zero crossings of a bipolar input (CO mode).

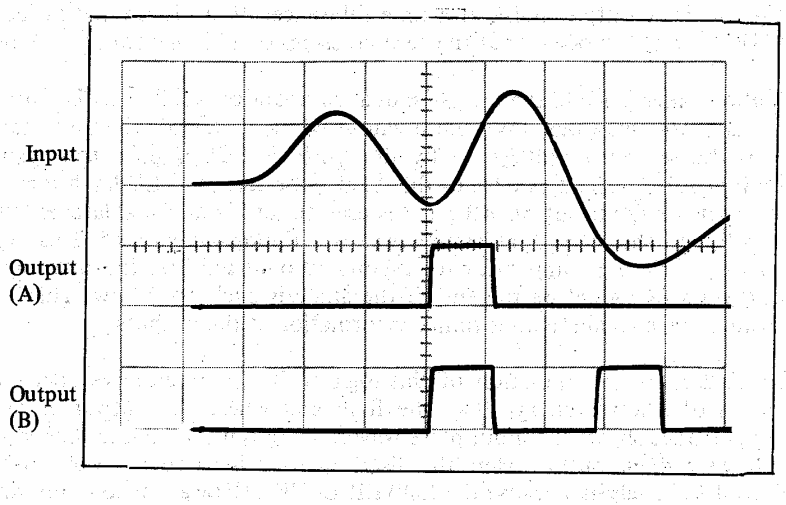
Pulse energy discrimination takes place in the precision dual comparator A6. The LLD output is taken at A6 pin 7, which yields a negative (logic low) pulse whose width represents the time span in which the input signal exceeds the reference voltage set by the LOWER LEVEL (E) front panel control acting thru buffer amplifier A9. The leading edge of this LLD pulse sets the LLD latch formed by A3a and A3b. As the latch is set, its $\overline{Q}$ output on A3 pin 3 is used to set 2 additional latches: one enables the ULD gate at A1 pin 9, and the other enables the crossover timing comparator. This logic scheme allows the ULD and crossover timing comparator to respond to only the first full pulse applied, and rejects any succeeding pulse arriving before the end of the analysis cycle to follow. This is a form of pileup rejection logic which prevents ambiguous timing information at the outputs.

The photograph below illustrates the operation of this logic with a representative piled up pulse in which the second pulse is of a lower energy than the first, and where the output pulse is set for minimum delay. The upper trace shows the input pulse waveform (a typical 0.5μsec shaped pulse pair) and the middle trace shows a single output. Here the discrimination is based upon the first lobe, and the second lobe is rejected for analysis because the LOWER LEVEL (E) was set to minimum, and the second lobe began before the first had recovered to the baseline. Using a higher setting of the LOWER LEVEL (E) control, the user can make the circuitry recognize the second lobe as a valid energy pulse despite the distorted energy peak due to pileup and improve the apparent pulse pair resolution. The lower trace then shows the output from this condition, a set of pulses each keyed to the constant fraction timing point.



Horiz.: 0.5μsec/div.

The photograph below illustrates another pileup condition in which the second lobe is higher than the first and the output pulse is delayed. Here the middle trace shows pileup rejection based upon the second lobe arriving during the analysis cycle of the first lobe, as well as being above the LOWER LEVEL (E). The lower trace shows how the second lobe is marginally accepted for analysis based upon the LOWER LEVEL (E) threshold being raised just above the valley between the peaks. Note that the use of the delayed output compromises the pulse pair resolution even for non-piled up pulses.



Horiz.: 0.5μsec/div.

The ULD output is taken at A6 pin 12, which yields a positive logic pulse whose width represents the time span in which the input signal may exceed the reference voltage provided by A8. The latter is a summing amplifier which forms the ULD reference from the sum of the LOWER LEVEL (E) and WINDOW (Δ E) control settings. The gating at A1 pins 9 and 10 allows a ULD trigger pulse to set the ULD latch formed by A1a and A1b only during the time span of the first LLD pulse: the enable of A1 pin 9 is removed at the end of the first LLD pulse seen at A6 pin 7 because the end of the latter resets the latch via A1d.

The contents of the LLD and ULD latches are held until interrogated later in the analysis cycle.

Crossover mode:

The second latch set by the LLD latch, and used as the enable for the crossover timing comparator, is formed in A4c and A4d. The $\overline{Q}$ output at A4 pin 11 is tied to the gate input of A11 at pin 4. The comparator A11 operates on the bipolar waveform zero crossing point, which is constant with variation of input signal and thus forms a stable time reference point. The comparator $\overline{Q}$ output on A11 pin 5 is used to reset the enable latch at A4 pin 9 so that again successive pulses or noise introduced at the input prior to completion of the analysis cycle underway do not cause erroneous multiple outputs, or affect the timing processes for the desired signal. The reset of the comparator enable signal is therefore used to trigger the delay one-shot A7. The delay provided covers 2 ranges: 0.1-1.1μsec, and 1-11μsec, each referenced to the $\overline{Q}$ output of the timing comparator A11.

At the end of the delay time, a second one-shot is initiated (A5 pin 13). This one-shot is set for 0.5μsec, to interrogate the LLD and ULD latches and form the SCA output as gated thru A2. As the 0.5μsec nominal pulse terminates, the reset one-shot at A5 pin 12 is generated. This logic low pulse is nominally 0.1μsec wide, and is used to reset the LLD and ULD latches (A3 pin 1, and A1 pin 1, respectively), thereby completing the analysis timing cycle.

Leading Edge mode:

In the leading edge mode, the timing comparator triggers at a low level threshold voltage below the setting of the LOWER LEVEL control. The output timing mark now triggers the reset one-shot (A5 pin 12) which clears any data in the ULD and LLD latches, and removes the comparator enable by resetting the enable latch at A4 pin 1. At the same time, the delay one-shot, A7, is triggered through the S3D contacts. At the end of the time out, the ULD and LLD latches are interrogated by A5 pin 13 as above, and yields the output as before. At the end of the 0.5 μsec strobe, the timing comparator enable latch is retriggered at A4 pin 5 to set the unit up for the next input pulse.

The + SCA output is provided as a positive logic output whose amplitude is adjustable by use of a socketed resistor, and whose pulse width is set by the interrogate pulse at A5 pin 13. The circuit is a variant on the standard totem pole configuration. When the AND gate at A2 pin 6, e.g., goes low, Q7 and Q9 are cut off, and Q8 sources the output pulse.

The – SCA output is derived by differentiating the start of the + SCA drive pulse for 20 nsec. The output circuit is a current steering differential amplifier with Q11 biased on, and Q10 cut off. The input negative pulse at A2 pin 6 is differentiated (C27) to cut off Q11 and allow Q10 to sink a measured 16 mA.